JVC

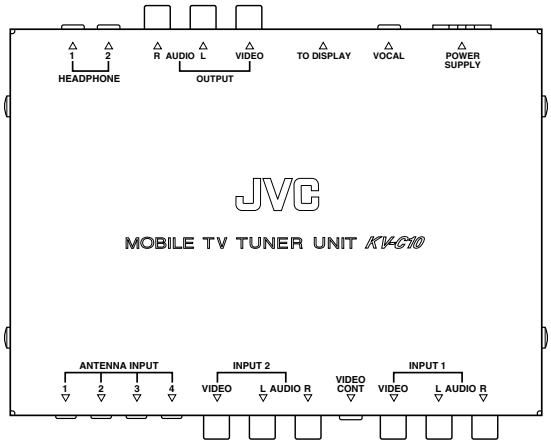
SERVICE MANUAL

MOBILE TV TUNER SYSTEM

KV-C10

Area Suffix

E ----Continental Europe



Contents

No.49655
Sep. 2001

Safety precaution

⚠ ***CAUTION*** **Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.**

Disassembly method

■Removing the metal cover

(See Fig.1)

1. Remove the four screws **A** attaching the metal cover on the back of the body.

2. Remove the four screws **B** attaching the metal cover on both sides of the body.

3. Remove the metal cover from the body by lifting the rear part of the cover.

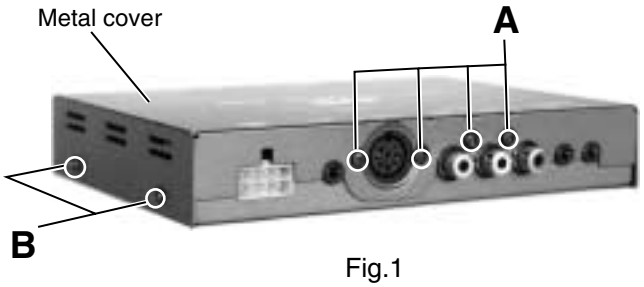


Fig.1

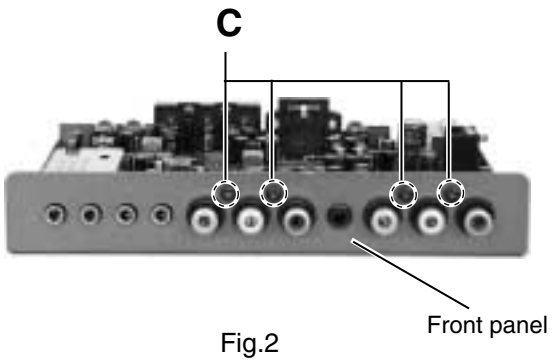


Fig.2

■Removing the main board

(See Fig.2 to 3)

・ Prior to performing the following procedure, remove the metal cover.

1. Remove the four screws **C** attaching the pin jack and the main board.

2. Remove the four screws **D** attaching the main board.

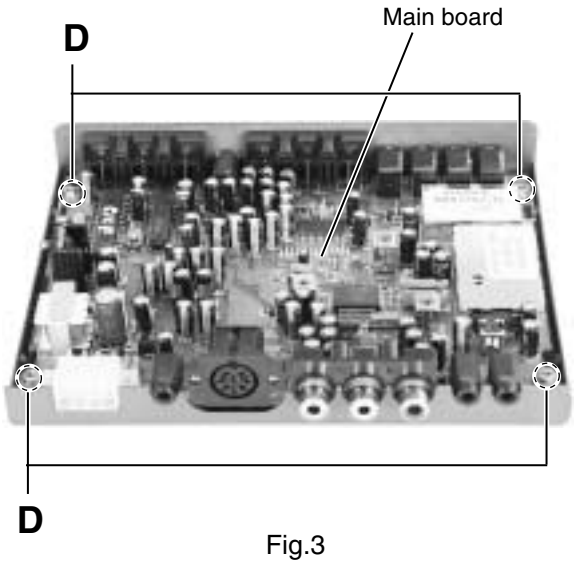


Fig.3

Adjustment method

1. Connection

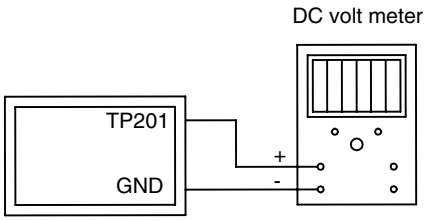


Fig. 1

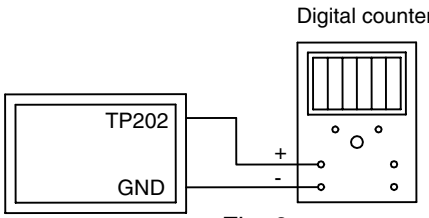


Fig. 2

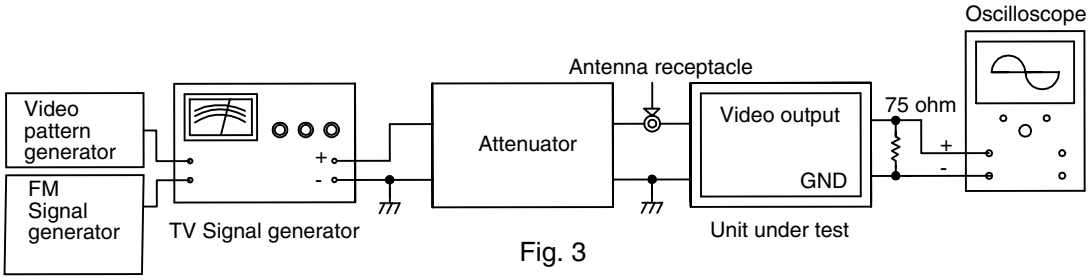


Fig. 3

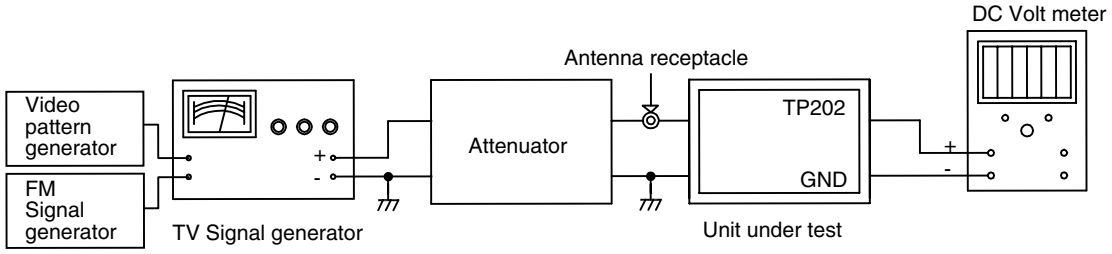


Fig. 4

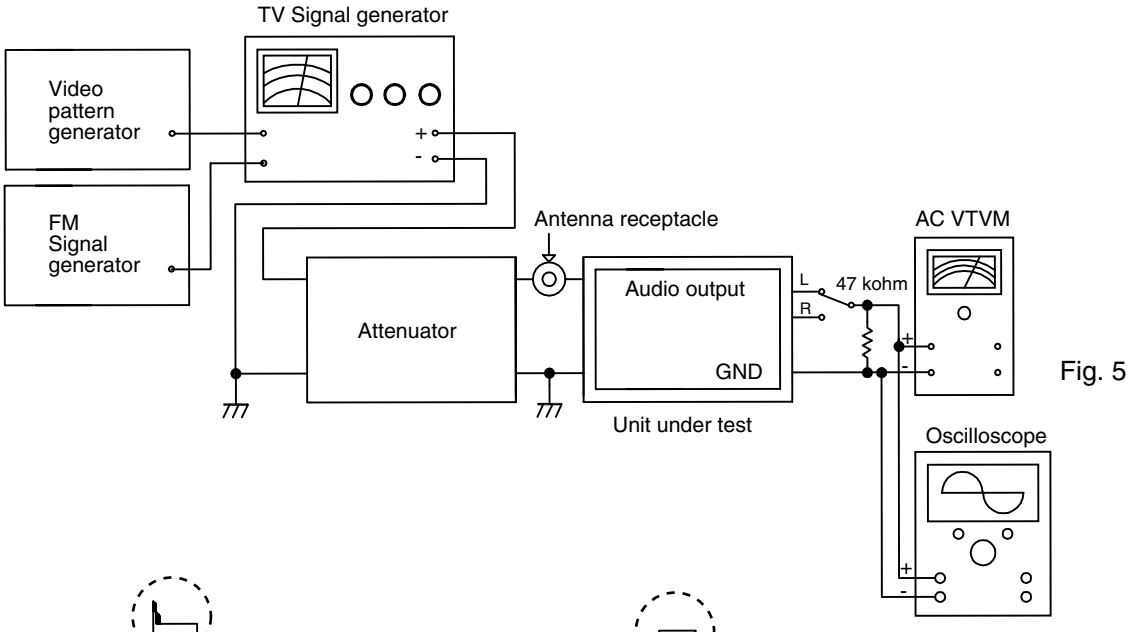


Fig. 5

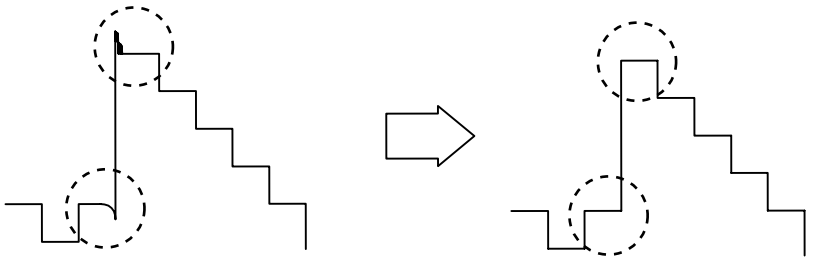


Fig. 6

2. Main board test point location

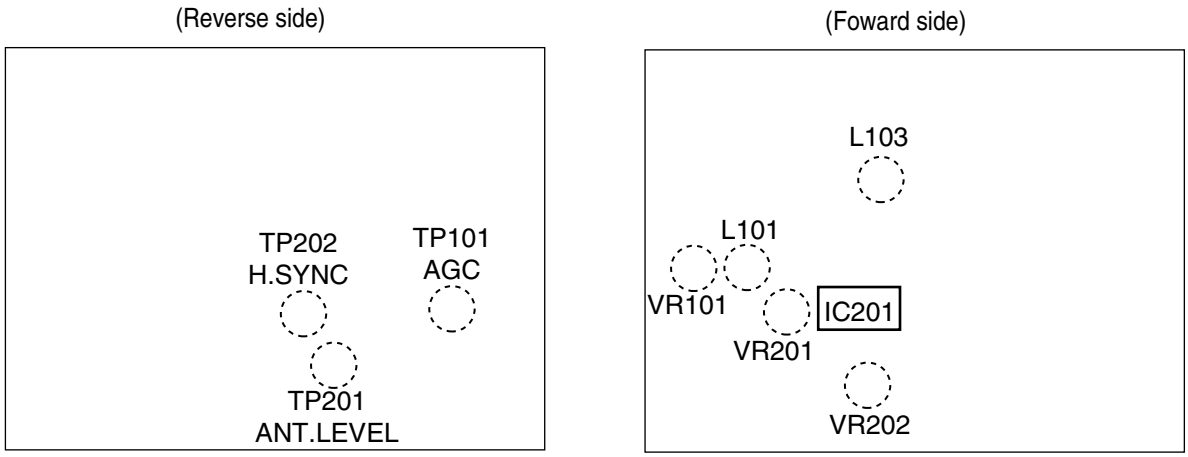


Fig. 7

3. Control settings

Power switch ---------- On
TV channel ---------- Center position
Video pattern generator ---------- Color bar

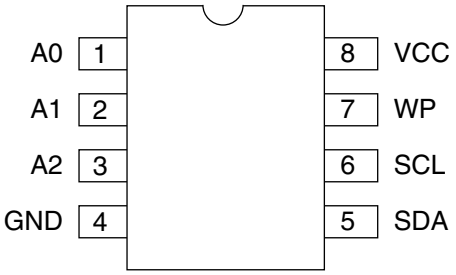
4. Adjust procedures

Step	Description	Connection	Signal generator	TV Channel	Test point	Adjustment
1	Antenna level adjustment	Fig. 1	—	—	TP201	Adjust VR202 for 1.3V
2	H.Sync adjustment	Fig. 2	—	—	TP202	Adjust VR201 for 15.63kHz
3	PIF coil adjustment	Fig. 3	Color bar Ch 12 60 dBuV	Ch 12	Video output	Adjust L101 for see Fig. 6
4	RF AGC Adjustment	Fig. 4	Color bar Ch 12 60 dBuV	Ch 12	TP101	Adjust VR101 for 3.5V
5	Audio adjustment	Fig. 5	Ch 12 60 dBuV	Ch 12	Audio output	Adjust L103 for max.output

Description of major ICs

■ AT24C04AN (IC502) : 2-Wire serial EEPROM

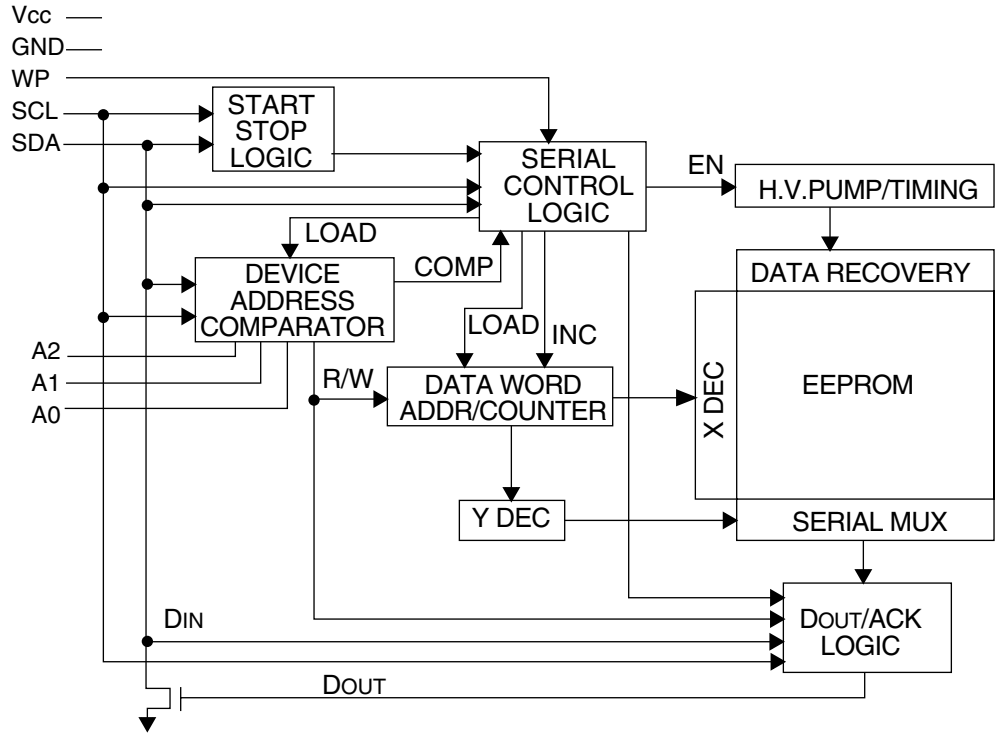
1. Pin layout



2. Pin function

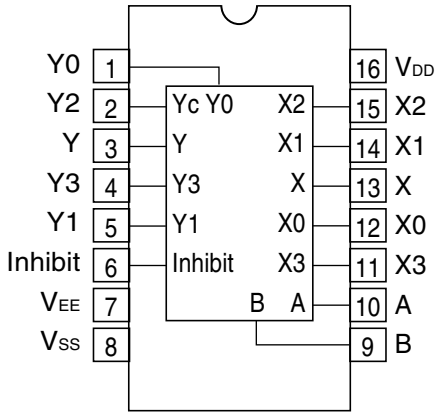
Pin No.	Symbol	Function
1~3	A0~A2	Address input
4	GND	Ground
5	SDA	Serial data
6	SCL	Serial clock
7	WP	Write protect
8	VCC	VCC

3.Block diagram

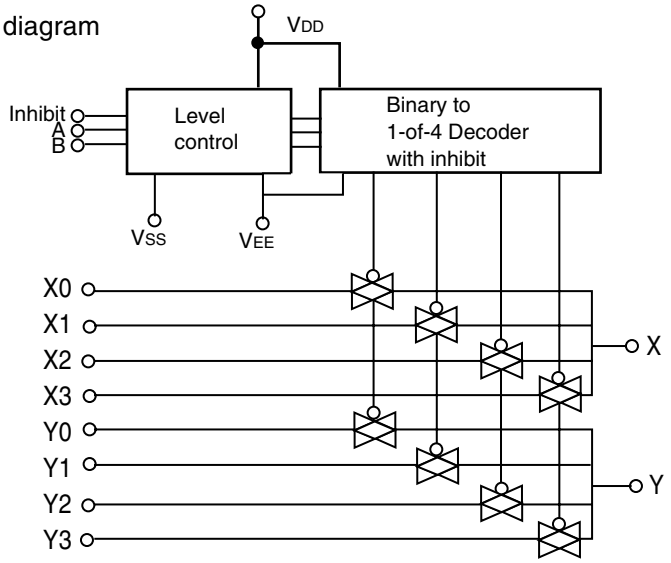


■ NJU4052B (IC302) : 4ch / 2ch Analog multiplexer

1.Pin layout

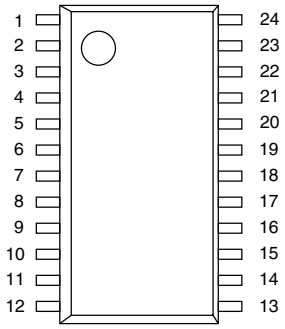


2.Block diagram



■ AN5290S (IC201) : Antenna diversity processor

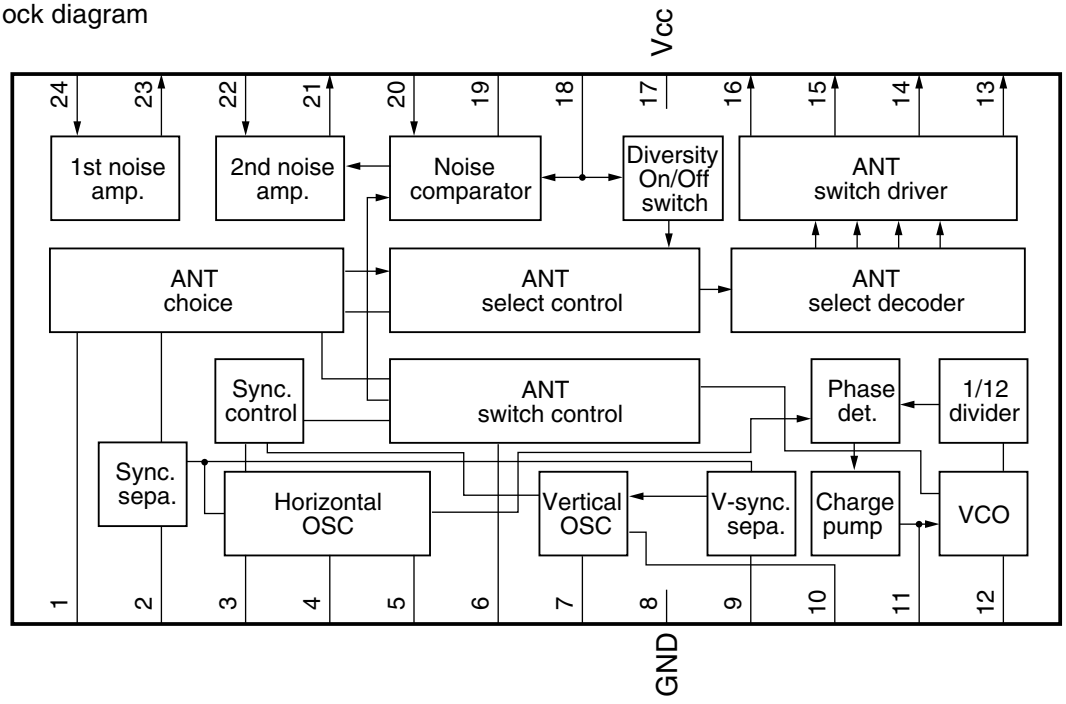
1. Pin layout



2. Pin function

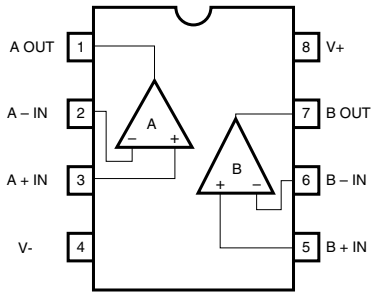
Pin No.	Function	Pin No.	Function
1	Antenna selection level holding capacitance	14	Antenna selection output 3
2	Sync. sepa. video signal input	15	Antenna selection output 2
3	Horizontal synchronizing signal AFC output	16	Antenna selection output 1
4	H-sync. setting oscillation time constant setting	17	Power supply
5	H-synchronizing signal output	18	Noise comparator level setting /diversity off
6	Output for noise canceler		
7	Vertical synchronizing signal output	19	Noise level hold capacitor
8	GND	20	Noise comparator input
9	V-sync. signal sepa. time constant setting	21	2nd noise amplifier output
10	V-sync. signal oscillation time constant setting	22	Video clamp input
11	Charge pump integral time-constant setting	23	1st noise amplifier output
12	VCO oscillation time-constant setting	24	Video signal input
13	Antenna selection output 4		

3. Block diagram

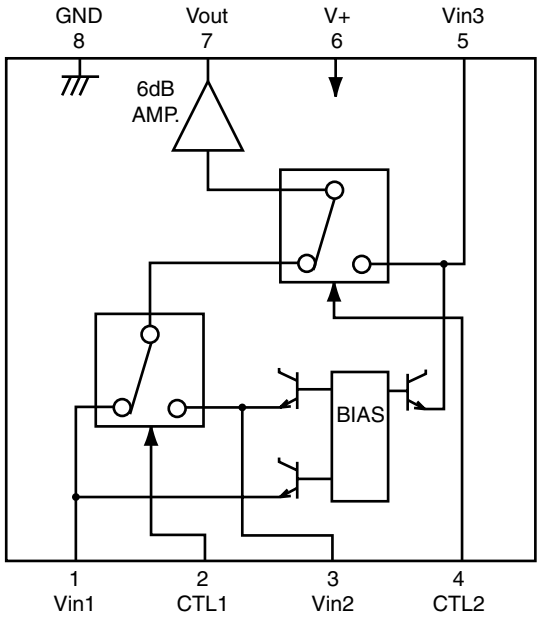


■ NJM4558M (IC303) : Op. amp.

1.Pin layout



■ NJM2246D (IC301) : Video switch

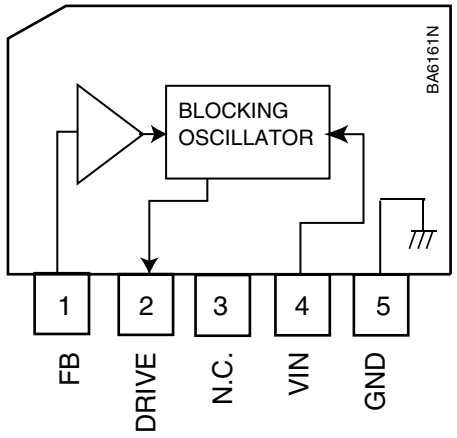


Control input - output signal

CTL 1	CTL 2	Output
L	L	VIN 1
H	L	VIN 2
L/H	H	VIN 3

■ BA6161N (IC102) : Switching regulator

1. Pin layout

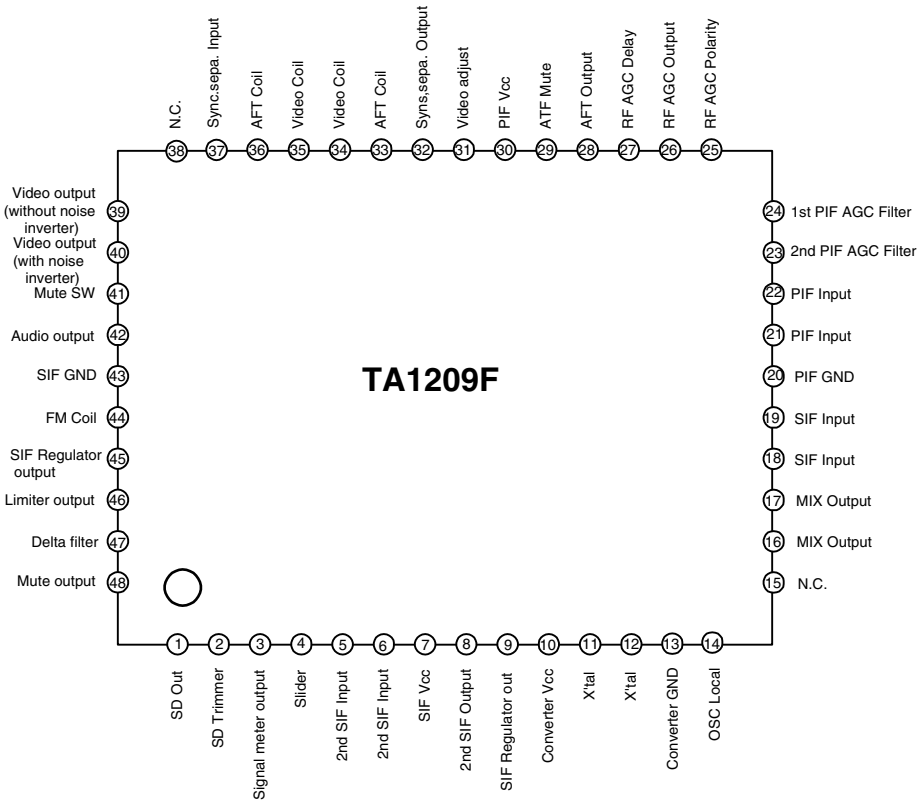


2. Pin function

Pin No.	Symbol	Function
1	FB	Feed back current return terminal
2	DRIVE	Transmission drive terminal
3	N.C.	Non connection
4	V_{IN}	Power supply input
5	GND	Ground

■ TA1209F (IC101) : TV converter

1. Pin layout



2. Pin function (1/3)

TA1209F

Pin No.	Symbol	I/O	Function
1	SD Output	O	SD Output terminal. (tuned : Hi, not tuned : Lo) This terminal is open collector output. Connect pull-up register.
2	SD Trimmer	-	Terminal to control SD sensitivity.
3	Signal meter output	O	Outputted DC voltage rises in proportion to input level.
4	Slider	-	According to resistance connected between this terminal and GND, controlling dc offset of #3 terminal is possible.
5	2nd SIF Input	I	2nd SIF input terminal. input 2nd SIF output signal through 10.7 MHz ceramic filter. Built-in matching register for ceramic filter (330 ohm).
6	2nd SIF Input	I	Bias terminal for 2nd SIF input. Connect capacitor between this terminal and GND.
7	SIF Vcc	-	SIF Vcc terminal (8.5V is recommended.)
8	2nd SIF Output		10.7 MHz 2st SIF signal is converted by Lo OSC signal is outputted.
9	SIF Reg. output	O	SIF Regulator output terminal (Typ. : 4.8V)
10	Convertor Vcc	-	Converter Vcc (8.5V is recommended.)

Pin function (2/3)

TA1209F

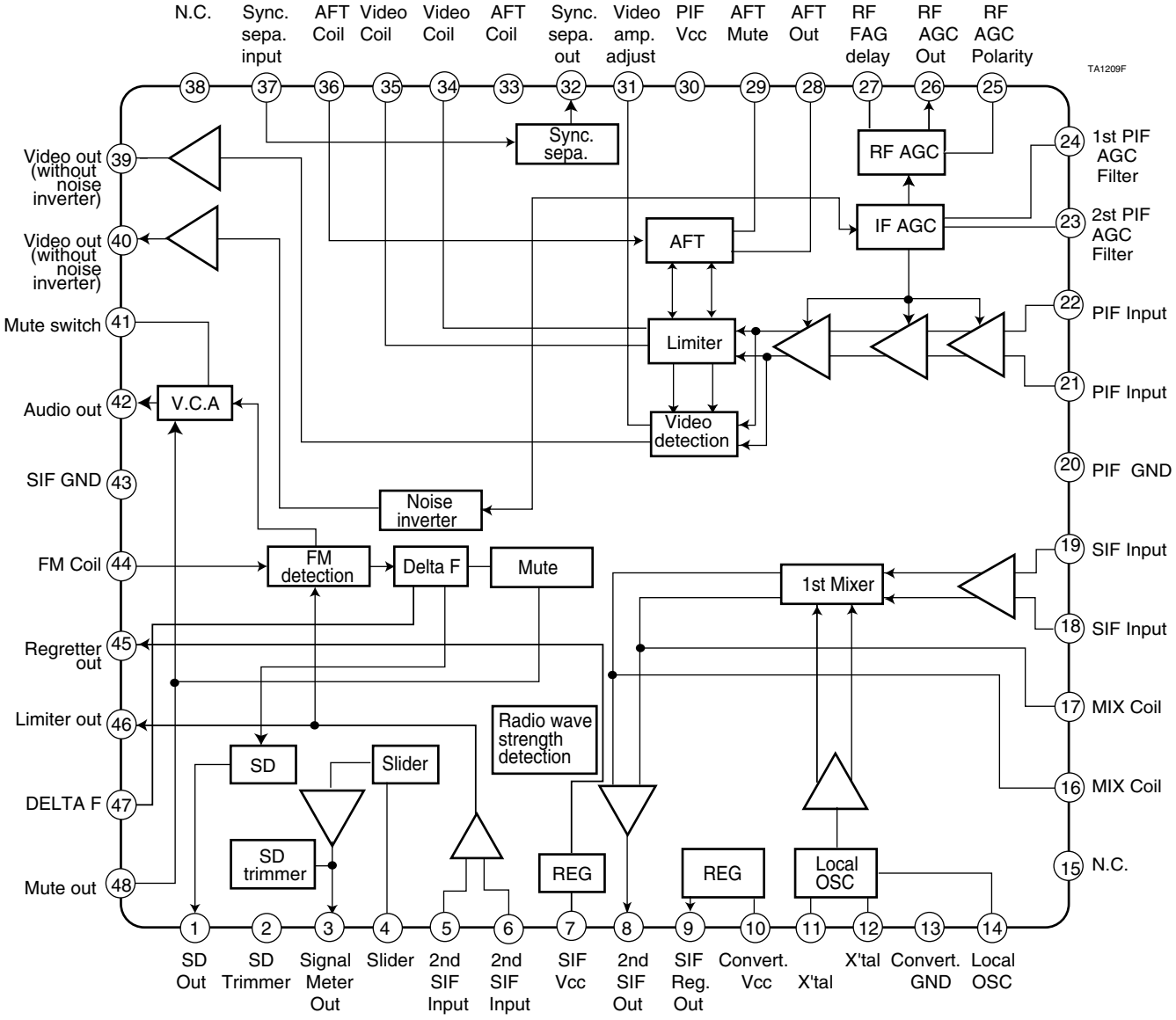
Pin No.	Symbol	I/O	Function
11~12	X'tal	-	Terminal for connecting crystal resonator to generate local OSC. signal.
13	Converter GND	-	Converter GND
14	Local OSC	-	Emitter of local circuit. Connect Register and capacitors.
15	N.C.	-	Non connection.
16~17	MIX Output	O	Mixer output terminal.
18~19	SIF Input	I	SIF Input terminal. (input impedance : 1.2 k ohm (Typ.))
20	PIF GND	-	PIF GND
21~22	PIF Input	I	PIF Input terminal. (input impedance : 5 k ohm (Typ.))
23	2ndPIF AGC Filter	-	Terminal to connect capacitor for PIF AGC responsibility, this IC is adopted dual time constant AGC circuit.
24	1nd PIF AGC Filter	-	Terminal to connect capacitor for PIF AGC responsibility, this IC is adopted dual time constant AGC circuit.
25	RF AGC Polarity	-	Terminal to switch RF AGC polarity. (open : reverse, GND : forward)
26	RF AGC Output	O	RF AGC Output terminal. (open-collector output)
27	RF AGC Delay	-	Changing comparator reference voltage adjusts RF AGC delay point.
28	AFT Output	O	AFT Detector output terminal based on double balanced multiplier.
29	AFT Mute	O	AFT Output is muted. when this terminal is connected to GND.
30	PIF Vcc	-	PIF Vcc terminal. (5 V is recommended.)
31	Video adjust	-	Video signal output voltage adjustment terminal. Changing this terminal voltage, it is possible to adjust video signal output voltage, to 1.0 Vp-p. (With no adjustment, video signal output voltage is 1 Vp-p(Typ.)) To prevent noise, connecting capacitor (0.01μ F) to GND is recommended.
32	Sync. sepa. Output	O	Sync, sepa. output terminal.
33	AFT Coil	O	Connect AFT detection coil.
34~35	Video coil	-	Connect video detection coil.
36	AFT Coil		Connect AFT detection coil.
37	Sync. sepa.Input	I	Sync, sepa. input terminal.
38	N.C.	-	Non connection
39	Video Output (Without noise inverter)	O	Video signal output terminal. Video signal without noise inverter is outputted, and can thus be used for diversity circuit, for example. Video output signal voltage is controlled by voltage of pin 4.
40	Video Output (With noise inverter)	O	Video signal output terminal. Video signal with noise inverter is outputted, Video output signal voltage is controlled by voltage of pin 4.

Pin function (3/3)

TA1209F

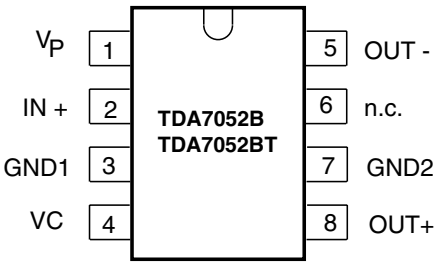
Pin No.	Symbol	I/O	Function
41	Mute SW	-	Audio mute SW. (open : mute on, GND : mute off)
42	Audio output	O	Audio signal output terminal.
43	SIF GND	-	SIF GND.
44	FM Coil	I	Connect FM coil. input limiter output signal through the coil for phase shift.
45	SIF Reg. output	O	SIF Regulator output terminal. (Typ. : 4.8V)
46	Limiter output	O	Limiter output terminal.
47	Delta F Filter	-	Connect capacitor for delta F circuit.
48	Mute output	O	DC voltage in proportion to input level is out putted. this voltage control audio mute.

3. Block diagram



■ TDA7052B(IC701, IC702) : Mono BTL audio amp. with DC volume control

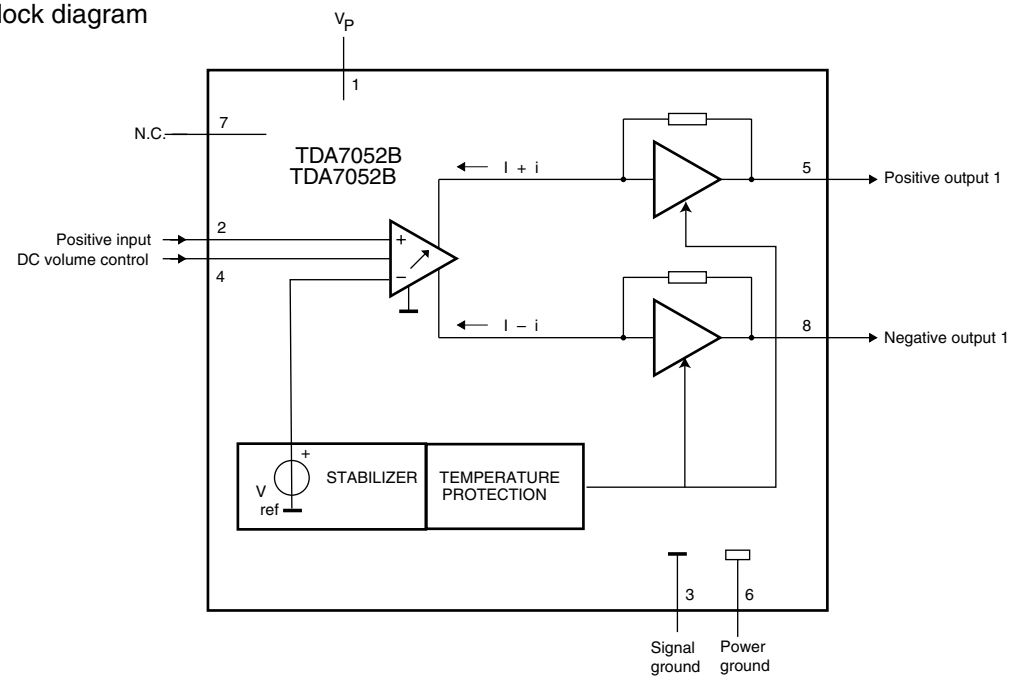
1. Pin layout



2. Pin function

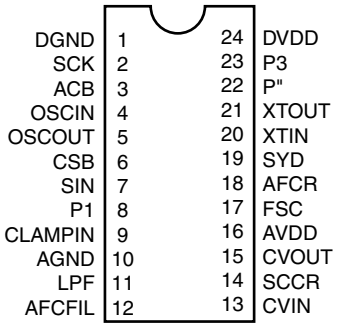
Pin No.	Symbol	Function
1	V_P	Positive supply voltage
2	IN+	Positive input
3	GND1	Ground
4	VC	DC volume control
5	OUT+	Positive output
6	n.c.	Not connected
7	GND2	Ground
8	OUT -	Negative output

3. Block diagram

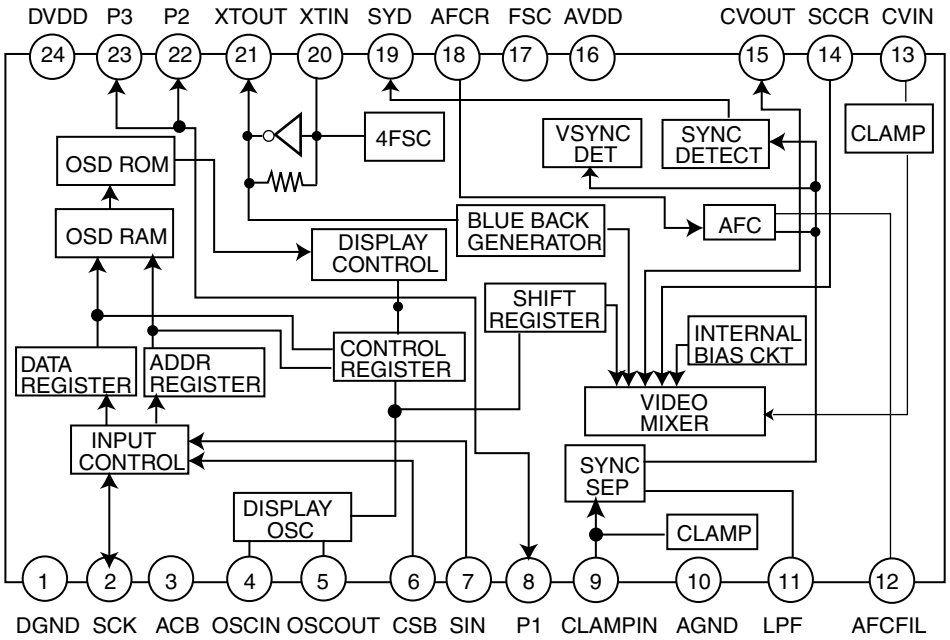


■ KS5514B-09 (IC401) : On screen display processor

1. Pin layout



2. Block diagram



3. Pin function

Pin No.	Symbol	I/O	Function
1	DGND	-	Digital ground
2	SCK	I	Serial clock input. When CSB pin is "L" then serial data is inputted by micom. Hysteresis input.
3	ACB	I	Auto clear pin/ if "L", then all circuit is reset. Built-in pull up resistor. Hysteresis input.
4	OSCIN	I	LC oscillation pin. Standard frequency is 7MHz & the horizontal start position is controlled by the clock of oscillation block.
5	OSCOUT	O	While pin 6 is low, serial data input is active.
6	CSB	I	Built-in pull up resistor.
7	SIN	I	Serial data input port pin. Built-in pull up resistor.
8	P1	O	General output port 1
9	CLAMPIN	I	Clamp input pin of composite video signal.
10	AGND	-	Analog ground.
11	LPF	-	Low pass filter.
12	AFCFIL	-	AFC filter output.
13	CVIN	I	Composite video signal input.
14	SOCR	I	SECAM chrome input.
15	CVOUT	O	Composite video output : 2 Vp-p.
16	AVDD	-	Analog VDD
17	FSC	I	FSC input (Not use)
18	AFCR	I	VCO oscillation frequency control.
19	SYD	O	When sync signal is inputted, then SYD is high.
20	XTIN	I	X-TAL
21	XTOUT	O	X-TAL
22	P2	O	General output port 2
23	P3	O	General output port 3
24	DVDD	-	Digital VDD

JVC

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